REMARKS

This responds to the Office Action mailed on June 27, 2007.

Claims 1, 7, 18, 24, 31 are amended, no claims are canceled, and no claims are added; as a result, claims 1-46 are now pending in this application.

§*103 Rejection of the Claims*

Claims 15-29, 31-34, 36-40, 42-45 were rejected under 35 U.S.C. § 103(a) as being unpatentable over WO 95/06285 to Petersen (hereinafter, "the Peterson reference") in view of U.S. Publication No. 2002/0107929 to Soussin *et al.* (hereinafter, "the Soussin reference").

Claims 1-8 and 12-14 were rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent 5,809,253 to Gallagher *et al.* (hereinafter, "the Gallagher reference") in view of the Petersen reference and the Soussin reference.

Claims 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the Gallagher reference in view of the Petersen reference and the Soussin reference as applied to claim 7, and further in view of U.S. Publication No. 2002/0167829 to Friedman *et al.* (hereinafter, "the Friedman reference).

Claim 11 was rejected under 35 U.S.C. § 103(a) as being unpatentable over the Gallagher reference, the Petersen reference, and the Soussin reference as applied to claim 7, and further in view of U.S. Publication No. 2001/0016877 to Dancs *et al.* (hereinafter, "the Dancs reference").

Claims 30, 35, 41 and 46 were rejected under 35 U.S.C. § 103(a) as being obvious over the Petersen reference in view of U.S. Publication No. 2001/0035845 to Zwern (hereinafter, "the Zwern reference") and the Soussin reference. Applicants disagree with the foregoing stated grounds of rejection and desire to further clarify various distinctions of the present invention over the cited art. Reconsideration of the present application is therefore requested in light of the present amendment and following remarks.

In the following discussion, the disclosed embodiments of the invention may be discussed in comparison to the prior art. It is understood, however, that any discussion of the disclosed embodiments, as well as any discussion of the differences between the disclosed embodiments of the present invention and the prior art do not define the scope or interpretation

of any of the claims. Instead, such discussed differences, if presented, are offered merely to help the Examiner appreciate important claim distinctions as they are discussed.

The Peterson reference discloses a data aligner that transfers data from an input having N+1 byte lanes to an output also having N+1 byte lanes. The disclosed data aligner includes a write data aligner and a read data aligner. With reference to Figure 1 and also to Table 1 in the Peterson reference, the write data aligner permits writing a fixed length word to a buffer from bytes of data received from a host data bus. The write data aligner is also operable to stack the data units received from the host so that no gaps occur. Similarly, the read data aligner is shown in Figure 2 of the Peterson reference. The read data aligner is configured to align data received from a buffer so that data units appear on data segment lanes of a host data bus in a manner specified by the host. In general, the data received from a buffer is arbitrarily aligned.

The Peterson reference does not disclose or suggest generating a header that is included with the data units. Moreover, the Peterson reference fails to disclose or to fairly suggest that a header portion may be positioned at various other locations within a data transaction. In contrast, the various embodiments of the present application disclose forming a header portion that may be sent along with the data in order to identify the data (page 16, 1st paragraph). For example, and with reference to Figure 5 of the present application, the first data being transferred includes a header 550, which is positioned in a lane 0, and additional headers may be positioned at other locations during the transaction. For example, in Figure 5, a header is also positioned in lane 1 following the first data transfer. Although the foregoing headers consume not more than a single lane, the header may also consume more than one lane, if desired.

The Examiner acknowledges that the Peterson reference does not disclose or suggest generating a header. Accordingly, the Examiner has cited the Soussin reference to provide this missing disclosure. The Soussin reference discloses a method of transmitting a message from a first computer to at least one second computer by introducing transmission information into a message header. The Examiner is referred to Figure 1 of the Soussin reference, which shows a network 4 having a plurality of computers (*e.g.*, computers 1, 2 and 3) that interact with the network 4. The disclosed message header 6 is attached to a body 7 of a message 5, as shown in Figure 2 of the Soussin reference. The header 6 includes at least one management instruction that may be inserted onto a message by a first computer. The header may be used to manage a

filing space within a second computer when the management instruction is executed by a second computer. The Examiner is referred to paragraph 7 of the Soussin reference.

Applicants therefore understand the Soussin reference to disclose a single header positioned before the body of a message that includes an executable instruction that cooperatively permits at least one other receiving computer to manage a filing space in the second computer. Soussin does not disclose, or suggest in any motivated fashion, positioning at least one header *within* a data block that is positioned between a first section and a second section in the data block.

Turning now to the claims, differences between the claim language and the applied references will be specifically pointed out. Claim 15 presently recites, in pertinent part: "An apparatus for assembling and sending data comprising...means for making a determination of how the local data and the downstream data will be sent over the communications bus, wherein making the determination includes...allocating one or more first contiguous lanes within a first section of a data block to at least some of the local data, wherein the data block comprises a set of multiple lanes, and each lane includes a set of configurable bits...allocating one or more second contiguous lanes within a second section of the data block to at least some of the downstream data, wherein the first section and the second section are contiguous...and...*positioning a header portion between the first section and the second section.*". (Emphasis added). The Peterson reference fails to disclose or suggest positioning a header between first and second sections . The Soussin reference fails to remedy this shortcoming since Soussin discloses positioning a header before a body of a message to be communicated to another computer. Claim 15 is therefore allowable over the cited combination. Claims depending from claim 15 are similarly allowable based upon the allowable form of the base claims and further based upon the additional limitations recited in the dependent claims.

Claim 18, as amended, recites in pertinent part: "An apparatus for sending data over a communications bus, the apparatus comprising...*providing a first header for the first source data and a second header for the second source data*...sending the first source data and the first header over the communications bus...identifying a first breakpoint corresponding to an end of the first source data...*sending the second source data and the second header over the communications bus, wherein the second header is positioned contiguously with the end of the*

first source data...". (Emphasis added). Again, the Peterson reference fails to disclose or suggest positioning a second header contiguously with the end of the first source data. The Soussin reference fails to remedy this shortcoming since Soussin discloses positioning a header before a body of a message to be communicated to another computer. Claim 18 is therefore allowable over the cited combination. Claims depending from claim 18 are similarly allowable based upon the allowable form of the base claims and further based upon the additional limitations recited in the dependent claims.

Claim 24, as amended, recites in pertinent part: "A method for sending data on a communications bus, the method comprising...arranging a first portion of first source data within a data block structure during a first processing period, wherein the data block structure includes a fixed number of contiguous, configurable bits and further wherein the first portion of the first source data includes a first header portion...arranging a first portion of second source data within a second section of the data block structure during the second processing period, wherein the second section is contiguous with the first section, and the second section includes a second set of contiguous bits, *wherein the first portion of the second source data includes a second header portion that is positioned between the first section and the second section...*". (Emphasis added). The Peterson reference fails to disclose or suggest this. Further, the Soussin reference fails to remedy this shortcoming since Soussin discloses only positioning a header before a body of a message to be communicated to another computer. Claim 24 is therefore allowable over the cited combination. Claims depending from claim 24 are similarly allowable based upon the allowable form of the base claims and further based upon the additional limitations recited in the dependent claims.

Claim 31, as amended, recites in pertinent part: "A method comprising...*generating at least one header*...allocating one or more first contiguous lanes within a first section of a data block to at least some of the first source data, wherein the data block comprises a set of multiple lanes, and each lane includes a set of configurable bits...allocating one or more second contiguous lanes within a second section of the data block to at least some of the second source data, wherein the second section begins at a next lane, which is contiguous with the first section...and...sending, over a communications bus and during a data block transmission period, the at least a portion of the first source data within the first section of the data block, and the at

least a portion of the second source data within the second section of the data block, *wherein the header is positioned between the at least some of the first source data and the at least some of the second source data.*". (Emphasis added). Yet again, the Peterson reference fails to disclose or suggest this. Further, the Soussin reference fails to remedy this shortcoming. Claim 31 is therefore allowable over the cited combination. Claims depending from claim 31 are similarly allowable based upon the allowable form of the base claims and further based upon the additional limitations recited in the dependent claims.

Claim 36 presently recites in pertinent part: "A method comprising...arranging first source data from a first source within a first section of a data block structure, wherein the first source data includes a first header portion, and wherein the data block structure includes a fixed number of contiguous, configurable bits, and data within the data block structure is periodically sent out on a communications bus...arranging the at least a portion of the second source data within the data block structure according to the indication, resulting in the at least a portion of the second source data occupying a second section of the data block that is contiguous with an end of the first section, *wherein the second header portion is positioned between the second section and the end of the first section...*". (Emphasis added). The cited combination of Peterson and Soussin fail to disclose or suggest this. Claim 36 is therefore allowable over the cited combination. Claims depending from claim 36 are similarly allowable based upon the allowable form of the base claims and further based upon the additional limitations recited in the dependent claims.

Claim 42 presently recites in pertinent part: "A method comprising...arranging first source data within a first section of a data block structure, *wherein the first source data includes a first header portion*, and wherein the data block structure includes fixed number of contiguous, configurable bits...receiving a request to send second source data over a communications bus, *wherein the second source data includes a second header portion*...identifying a location of a breakpoint in the first source data...arranging at least a portion of the second source data within a second section of the data block structure after the breakpoint, wherein the second section is contiguous with an end of the first section...and...sending the first source data and the at least a portion of the second source data over the communications bus during a data block transmission period.". (Emphasis added). Again, the cited combination of Peterson and Soussin fail to

disclose or suggest this. Claim 42 is therefore allowable over the cited combination. Claims depending from claim 42 are similarly allowable based upon the allowable form of the base claims and further based upon the additional limitations recited in the dependent claims.

Turning now to the rejection of claims 1-8 and 12-14, the Examiner has cited the Gallagher reference for disclosing, *inter-alia*, a processor and multiple memory modules. Applicants note that the Gallagher reference fails to disclose, or to fairly suggest positioning a header between at least some of the first source data and at least some of the second source data. Further, as discussed in greater detail above, the Peterson and Soussin references also fail to disclose this.

Returning again to the claim language, specific differences between the applied references and the claim language will be specifically pointed out. Claim 1, as amended, recites in pertinent part: "An electronic system comprising...a processor...multiple memory modules, operatively coupled together through a communications bus, which return data requested in the one or more memory access requests, wherein each of the multiple memory modules is a data source, and a memory module of the multiple memory modules...*generates a header for at least one of the first source data and the second source data*...and...sends, over the communications bus and during a data block transmission period, the at least a portion of the first source data within the first section of the data block, and the at least a portion of the second source data within the second section of the data block, *wherein the header is positioned between the at least some of the first source data and the at least some of the second source data.*". (Emphasis added). The cited combination still fails to disclose this. Claim 1 is therefore allowable over the cited combination. Claims depending from claim 1 are similarly allowable based upon the allowable form of the base claims and further based upon the additional limitations recited in the dependent claims.

Claim 7, as amended, recites in pertinent part: "A memory module comprising...one or more memory storage units for storing local data..and...a hub, operatively coupled to the one or more memory storage units and to a communications bus over which the hub can receive downstream data from one or more other hubs, wherein the hub...determines that first source data and second source data are available... *generates a header for at least one of the first source data and the second source data*...and...sends, over the communications bus and during

a data block transmission period, the at least a portion of the first source data within the first section of the data block, and the at least a portion of the second source data within the second section of the data block, *wherein the header is positioned between the at least a portion of the first source data and the at least a portion of the second source data.* ". (Emphasis added). Again, the cited combination still fails to disclose this. Claim 7 is therefore allowable over the cited combination. Claims depending from claim 7 are similarly allowable based upon the allowable form of the base claims and further based upon the additional limitations recited in the dependent claims.

With respect to the Examiner's rejections based upon the Freidman, dancs and Zwern references, Applicants respectfully submit that the foregoing references still do not remedy the shortcomings present in the Peterson, Soussin and Gallagher references.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

CONCLUSION

Applicants respectfully submit that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicants' attorney at (612) 349-9587 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 27th day of September 2007.

Amy Moriarty
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Signature